THAT WHICH IS CLAIMED IS:

1. A method for amplifying with pre-emphasis a digital signal (A) representative of a datum (DATUM) to be transmitted by a line driver with pre-emphasis, the gain of which varies from a certain upper value to a certain lower value and vice versa, comprising the steps of:

varying the gain of said driver with pre-emphasis by setting it to said upper value in coincidence with the switchings of said digital signal (A) and reducing it to said lower value in absence of switchings of the digital signal,

characterized in that said gain variation is performed as follows:

amplifying said digital signal (A) with a first gain (M) generating an amplified replica signal (M*A);

delaying said digital signal (A) of a certain pre-established time (TBIT), generating a delayed replica signal (B);

amplifying said delayed replica signal (B) with a second gain (N) generating a delayed and amplified replica signal (N*B);

outputting over said line a signal (OUT) correspondent to the difference between said amplified replica signal (M*A) and said delayed and amplified replica signal (N*B).

2. The method of claim 1, wherein said delay (TBIT) is equal to a duration of a bit pulse of said digital signal (A).

3. The method of claim 1, wherein said delay (T_{BIT}) is a fraction of a duration of a bit pulse of said digital signal (A).

4. A line driver with pre-emphasis of a digital signal (A) representative of a datum (DATUM)to be transmitted over an output line, comprising

a driver with pre-emphasis the gain of which may vary from a pre-established upper value to a lower value and vice versa, being input with said digital signal (A), and producing an output signal (OUT) by amplifying said digital signal (A) with a gain equal to said upper value in coincidence with switchings of said signal (A) and is equal to said lower value in absence of switchings of the digital signal (A),

characterized in that it comprises

an input circuit providing a replica signal (B) of said digital signal (A) delayed by a certain pre-established time (T_{BIT}),;

said driver with pre-emphasis producing said output signal (OUT) as the difference signal between an amplified replica (M*A) with a first gain (M) of said digital signal (A) and an amplified replica (N*B) with a second gain (N) of said delayed replica signal (B).

5. The line driver with pre-emphasis of claim 4, wherein said input circuit determining two input signal paths respectively for the input signal and for an inverted replica thereof, each path including:

a D-type flip-flop clocked by an externally generated timing signal (CK), input with said datum (DATUM) or the inverted replica thereof and generating said digital signal (A) or an inverted replica thereof

(AN);

a delay circuit of a pre-established interval (TBIT) of said digital signal (A) or of the inverted replica thereof (AN), generating said delayed replica signal (B) or an inverted replica thereof (BN);

said driver with pre-emphasis comprises a pair of standard LVDS cells first and second with output nodes connected in common and generates said output signal (OUT) as a differential pair of output signals (VO, VON), said first LVDS cell being driven by said digital signal (A) and by the inverted replica thereof (AN), said second LVDS cell being driven by said delayed replica signal (B) and by the inverted replica thereof (BN), the bias currents of said first cell and of said second cell being equal to the ratio (M/N) between said gains first (M) and second (N).

6. The line driver with pre-emphasis of claim 5, wherein said delay circuit is composed of another D-type flip-flop in cascade to said first flip-flop.

7. The line driver with pre-emphasis of claim 5, wherein said timing signal (CK) is a clock signal used for generating said digital signal (A).

8. The line driver with pre-emphasis of claim 5, wherein the frequency of said timing signal (CK) is multiple of the frequency of a clock signal used for generating said digital signal (A).